IN THE TITLE

Please amend the title as follows:

Clock System for Reproducing Apparatus and Method

IN THE SPECIFICATION

Please amend the paragraph starting on page 4, line 11 and ending on page 5, line 3 as follows:

To accomplish the above object, according to the invention [[of Claim 1]], there is provided a reproducing apparatus in which a first reproduction signal and a second reproduction signal are simultaneously obtained by a plurality of reading means from a disc-shaped recording medium on which data of a high-transfer rate and data of a low-transfer rate have been recorded, comprising: signal layout converting means for time division multiplexing the first reproduction signal and the second reproduction signal and arranging them; sync adjustment information forming means for forming sync adjustment information which is optimum to each reproduction signal from the first reproduction signal and the second reproduction signal; waveform equalizing means for executing a waveform equalizing process to an output of the signal layout converting means; switching means for switching characteristics of the waveform equalizing means in accordance with the sync adjustment information; and a PLL for generating a clock signal according to the sync adjustment information.

Please amend the paragraph on page 5, lines 4-23 as follows:

According to the invention ~~of Claim 6 of the invention~~, there is provided a reproducing method whereby a first reproduction signal and a second reproduction signal are simultaneously obtained by a plurality of reading means from a disc-shaped recording medium on which data of a high-transfer rate and data of a low transfer rate have been recorded, comprising: a signal layout converting step of multiplexing the first reproduction signal and the second reproduction

signal and arranging them; a sync adjustment information forming step of forming sync adjustment information which is optimum to each reproduction signal from the first reproduction signal and the second reproduction signal; a waveform equalizing step of executing a waveform equalizing process to an output of the signal layout converting means; and a step of switching characteristics of the waveform equalizing step in accordance with the sync adjustment information, inputting an output signal of the waveform equalizing step to a PLL, and generating a clock signal according to the sync adjustment information.

Page 7, please amend the second paragraph, lines 15-22 as follows:

An Ach head 3 reproduces the front surface of the disc 1 and, at the same time, a Bch head 4 reproduces the back surface of the disc 1. The Ach head 3 and the Bch head 4 read the data of the high-transfer rate and the data of the low-transfer rate. A first reproduction signal read by the Ach head 3 is supplied to a preamplifier [[5]] 6. A second reproduction signal read by the Bch head 4 is supplied to a preamplifier [[6]] 5.

Page 9, please amend the second paragraph, lines 13-24 as follows:

The clock extracting unit 11 is an internal signal generating circuit corresponding to the high-transfer rate and the low-transfer rate. An example of an internal construction of the clock extracting unit 11 will be described hereinbelow. The output signal from the FIFO buffer of the signal layout converting circuit 9 is first supplied to a waveform equalizing circuit 16 in the clock extracting unit 11. The waveform equalizing circuit 16 is constructed by: a high pass filter (hereinafter, abbreviated to HPF) unit 12; an adder 28; an RF amplifier 13; a low pass filter (hereinafter, abbreviated to LPF) unit 14; and a binary limiter circuit (LIM) 15.